Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-14 (canceled)

Claim 15. (new) A delay lock loop apparatus for use with an externally generated clock signal comprising:

a delay device comprising a first delay element and a second delay element, wherein the first delay element is configured to generate a first output responsive to a control signal and a first input, and wherein the second delay element is configured to generate the first input responsive to the externally generated clock signal and a set signal related to the frequency of the externally generated clock signal,

a feedback device operably connected to the first delay element and configured to generate a time delayed first output,

a phase difference detection device configured to generate signal responsive to the phase difference between the time delayed first output and the externally generated clock signal, and

a frequency detection unit configured to generate the set signal responsive to the frequency of the externally generated clock signal.

Claim 16. (new) The apparatus of claim 15, wherein the first delay element is responsive to a filtered control signal, and wherein the apparatus further comprises,

a filtering device operably connected to the phase difference detection device and the first delay element.

Claim 17. (new) The apparatus of claim 15, wherein the feedback device is farther configured to generate the time delayed first output determined based upon a receiver time delay and a driver time delay.

Claim 18. (new). The apparatus of claim 15, wherein the second delay element is configured to generate the first input responsive to a first set signal related to a first external clock frequency, the device further comprising,

a third delay element configured to generate the first input responsive to a second set signal related to a second external clock frequency.

Claim 19. (new) The apparatus of claim 15, wherein the delay device comprises a controllably variable capacitor element.

Claim 20. (new) The apparatus of claim 15, wherein the delay device comprises a controllably variable current inverter.

Claim 21. (new) The apparatus of claim 15, wherein the delay device comprises an inverter chain.

Claim 22. (new) A method of providing clock signals to a circuit, the method comprising the steps of:

providing a delay control apparatus comprising a first variable delay element and at least one frequency variable delay element,

detecting the frequency of an external clock signal,

adjusting the time delay of the at least one frequency variable delay element based upon the frequency of the external clock signal,

delaying the external clock signal with the at least one frequency variable delay element and providing the delayed external clock signal to the first variable delay element,

further delaying the delayed external clock signal with the first variable delay element,

providing the further delayed external clock signal to a feedback device,

time delaying the further delayed external clock signal with the feedback device,

detecting the phase difference between the time delayed external clock signal and the external clock signal,

generating a control signal based upon the detected phase difference, and

controlling the time delay of the first variable delay element with the control signal so as to reduce the detected phase difference.

Claim 23. (new) The method of claim 22, wherein the step of detecting the frequency of an external clock signal comprises the step of:

detecting the frequency of an external clock signal over a predetermined number of frequency cycles.

Claim 24. (new) The method of claim 23, wherein the step of detecting the frequency of an external clock signal over a predetermined number of frequency cycles comprises the step of

detecting the frequency of an external clock signal over eight frequency cycles.

Claim 25. (new) The method of claim 22, further comprising, before the step of detecting the frequency of an external clock signal, the step of:

resetting the delay control apparatus with a reset pulse.

Claim 26. (new) The method of claim 22, wherein the step of providing at least one frequency variable delay element comprises the step of

providing a first frequency variable delay element responsive to control signals related to a first frequency and a second frequency and not responsive to control signals related to a third frequency, and

providing a second frequency variable delay element responsive to control signals related to the second frequency and the third frequency and not responsive to control signals related to the first frequency.

Claim 27. (new) The method of claim 22, wherein the step of time delaying the further delayed external clock signal comprises the steps of,

providing a receiver and a driver,

determining the receiver time delay,

determining the driver time delay, and

time delaying the further delayed external clock signal by an amount of time equal to the receiver time delay plus the driver time delay.

Claim 28. (new) The method of claim 22, further comprising the steps of;

providing a filtering device, and

filtering the generated control signal.